REMARKS/ARGUMENTS

Claims 1, 6, 7, 9-15, 17, 18, 20-27, 44, 52, 58, and 61-77 were pending in this application. Claims 1, 7, 11, 12, 15, 17, 21, 25, 44, 61, 68, and 75-77 have been amended. Claims 14 and 24 have been canceled. Accordingly, claims 1, 6, 7, 9-13, 15, 17, 18, 20-23, 25-27, 44, 52 58, and 61-77 presently are pending.

The Examiner's courtesy in conducting a personal interview with applicant's representative is acknowledged with appreciation.

Claims 1, 6, 7, 9, 14, 17, 18, 20, 24, 26, 44, 61, 68, and 75-77 stand rejected under 35 U.S.C. §102(b) as being anticipated by Nishizawa et al., U.S. Patent No. 5,275,184. Applicant respectfully traverses the rejection.

The present invention relates to a method for reducing surface contaminants from the air/liquid interface in a wet etching bath. As such, amended independent claim 1 recites a "method for removing surface contaminants from an air/liquid interface" by "reducing an overall volume of a semiconductor processing fluid" in a processing bath by "rapidly displacing an upper portion of the semiconductor processing fluid" present in the bath "while said wafers remain immersed in a lower portion of said semiconductor processing fluid," "to remove said surface contaminants from said air/liquid interface." Similarly, amended independent claim 7 recites a method for "reducing the contamination on a semiconductor wafer" by "rapidly reducing a volume" of a wet etching bath by "removing a substantial portion of an upper portion of said etching fluid from said wet etching bath to remove surface contaminants from an air/liquid interface of said wet etching bath, while retaining said semiconductor wafer in a lower portion of said etching fluid," and "subsequently removing said semiconductor wafer from said wet etching bath."

Amended independent claim 17 recites a method for etching a semiconductor wafer with "an aqueous hydrofluoric acid" etching fluid, a volume of which is reduced by "rapidly removed a portion of said etching fluid from the upper surface of said etching fluid

to reduce an overall volume of fluid contained in said wet etching vessel," "while keeping said semiconductor wafer immersed in a remaining portion of said etching fluid."

Independent claim 61 recites a "method for removing surface contaminants from an air/liquid interface of a semiconductor processing bath" that includes "reducing a volume of said semiconductor processing bath contained within a processing apparatus" by "rapidly removing an upper portion of a semiconductor processing fluid present in said processing apparatus" "while said wafers are in a remaining lower portion of said bath" "to reduce an overall volume of fluid contained within said processing apparatus" and thereby "break eddy currents holding said surface contaminants at said air/liquid interface."

Independent claim 68 recites "reducing a volume of said semiconductor processing bath in a processing vessel" by removing rapidly "an upper portion of a semiconductor processing fluid present in said processing vessel," "while said wafers are in a remaining lower portion of said processing vessel," "to reduce an overall volume of fluid in said processing vessel."

Independent claim 75 recites a "method for reducing the contamination on a semiconductor wafer" processed in a wet etching bath by "reducing a volume of etching fluid in said wet etching bath" and "breaking eddy currents of said wet etching bath by rapidly removing an upper portion of said etching fluid from a processing vessel containing said wet etching bath to reduce an overall volume of fluid contained within said processing vessel," the "act of breaking said eddy currents further releasing surface contaminants which are formed at an air/liquid interface of said wet etching bath and held at said air/liquid interface by said eddy currents."

Independent claim 76 recites a "method for reducing the contamination on a semiconductor wafer" processed in a wet etching bath containing etching fluid by "reducing a volume of said wet etching fluid" and "breaking surface tension forces of said wet etching bath by rapidly removing an upper portion of said etching fluid from a processing vessel containing said wet etching bath, said act of breaking said surface tension forces further releasing surface contaminants which are formed at an air/liquid interface of

said wet etching bath and held at said air/liquid interface by said eddy currents," and subsequently "removing said semiconductor wafer from said wet etching bath."

Claim 77 recites a method for "reducing the contamination on a semiconductor wafer" which includes "processing said semiconductor wafer in a static etching bath containing an etching fluid' and "reducing a volume of said etching fluid by rapidly removing an upper portion of said etching fluid from a container holding said static etching bath to reduce an overall volume of fluid contained within said container" "while said semiconductor wafer is in a remaining portion of said static etching bath."

In contrast to the present invention, Nishizawa et al. teaches a wafer treating system in which a volume of treating fluid is maintained at a constant level. Nishizawa et al. does not teach or suggest rapidly removing fluid to reduce an overall volume of fluid within a treatment container or apparatus, as recited in the present claims. On the contrary, in Nishizawa et al., the volume of fluid in the bath remains constant as "old treatment solution inside the container is rapidly displaced by the new treatment solution" (col. 3, lines 54-55). Moreover, the flow of fluid is laminar according to the Nishizawa et al. disclosure. The claims respectfully are submitted as being patentable over Nishizawa et al.

Claims 10, 27, 62 and 69 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nishizawa et al. in view of Itoh et al., U.S. Patent No. 5,795,401.

The claimed invention would not have been obvious over Nishizawa et al. in view of Itoh et al. As noted above, Nishizawa et al. is silent about the reduction in volume of a treating bath, and also is silent regarding rapid removal of "surface contaminants" or of "surface contaminants from an air/liquid interface" by opening a valve, hingedly releasing a door, sliding a door, or telescopically collapsing sidewalls of a vessel containing an etching bath. Itoh et al. recites using a "paddle," (discussed further below) but does not teach or suggest reducing the volume of a treating bath, or removal of any contaminants from the etching bath, much less to the removal of "surface contaminants from an air/liquid interface." Itoh et al. merely refers to the scrubbing of a wafer surface using a rotary brush

while pressure is applied by jetting a fluid on the other surface of the wafer. In addition, Itoh et al. does not teach or suggest rapidly removing a substantial portion of the etching liquid. Itoh et al. does not even mention an etching fluid. Itoh et al. refers only to a wash liquid that is purified water and that comes into contact with a rotary brush that cleans the wafer surface. Thus, there is no teaching or suggestion in either of these two references for the claimed subject matter.

Further, Applicant respectfully submits that the proposed combination of references lacks the motivation required for a *prima facie* rejection under 35 U.S.C. § 103. Nishizawa et al. refers to wafer surface treatment by using at least two different solutions. Nowhere does Nishizawa et al. disclose or suggest reducing a volume of the treatment bath. Itoh et al. does not cure the deficiencies of Nishizawa et al., referring only to the actual physical cleaning and scrubbing of the wafer surface by mechanical means such as a cylindrical rotary brush. The back pressure "paddle" 7 disclosed by Itoh et al. is not analagous to the paddle recited in the claims of the present invention. On the contrary, paddle 7 disclosed by Itoh et al. is a fluid jet device that discharges an inert gas or high purity water as the back pressure fluid. Itoh et al. does not teach or suggest a paddle such as that disclosed and described in the present application which is utilized to reduce the volume of a treatment bath, as shown in Fig. 15, for example. Thus, the proposed combination appears to be based on picking and choosing selected portions of each reference, without regard to the totality of teachings of the references, in an improper attempt to reconstruct the invention using hindsight. Accordingly, a person of ordinary skills in the art could not have been motivated to combine Nishizawa et al. with Itoh et al.

Further, Applicants submit that the proposed combination, even if properly combinable, fails to achieve the claimed invention. For example, the "paddle" disclosed in Itoh et al. will not reduce treatment bath volume as recited in the present claims. Claims 10, 27, 62, and 69 respectfully are submitted as being patentable over the cited Nishizawa et al. and Itoh et al. references.

Claims 11, 21, 63 and 70 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nishizawa et al., in view of Mohindra et al., U.S. Patent No. 5,958,146.

Amended independent claim 11 recites "a method for removing surface contaminants from an air/liquid interface of a semiconductor processing etching bath for processing semiconductor wafers." The method includes "reducing a volume of said semiconductor processing bath contained within a processing apparatus by rapidly removing from said processing apparatus an upper portion of a semiconductor processing fluid present in said bath," "to rapidly reduce an overall volume of processing fluid contained within said processing apparatus, while said wafers are in said bath, by opening a valve in said bath to remove said surface contaminants from said air/liquid interface." Amended claims 21 recites a method for etching a semiconductor wafer.

Amended independent claim 21 recites a method for etching a semiconductor wafer. The method includes "placing an etching fluid into a wet etching vessel" and "placing said semiconductor wafer in said etching fluid," then "contacting said semiconductor wafer with said etching fluid for a predetermined time," and "reducing a volume of said etching fluid by rapidly removing a portion of said etching fluid from the upper surface of said wet etching vessel by opening a valve to reduce rapidly an overall volume of fluid in said wet etching vessel while said semiconductor wafer remains in a lower portion of said etching fluid."

As noted above, Nishizawa et al. does not teach or suggest removing surface contaminants by "reducing a volume of said semiconductor processing bath" by "rapidly removing an upper portion of a semiconductor processing fluid present in said bath" "to rapidly reduce an overall volume of processing fluid contained within said processing apparatus, while said wafers are in said bath. Further, Nishizawa et al. does not teach that the removal is accomplished by "opening a valve in said bath," as recited in the present invention.

Mohindra et al. does not cure the deficiencies of Nishizawa et al. Mohindra et al. discloses a cleaning technique for a semiconductor wafer that uses a hot or heated liquid

in conjunction with a carrier gas which includes a cleaning enhancement substance. Mohindra discloses the use of control valves in the method of cleaning the semiconductor wafers, and the Office Action points out that "it would have been obvious to one ordinary skill in the art . . . to have provided Nishizawa et al. reference with a valve as taught by Mohindra et al. because the use of valve would have provided another method of removing contaminants from the top of the wafer etching bath." Although several control valves, and a drain valve 236, are disclosed, Mohindra et al. does not teach or suggest that any of the valves is used for the reducing volume of a treatment bath for rapid removal of "surface contaminants from an air/liquid interface" of an upper portion of the etching fluid, as in the claimed invention. Accordingly, there is nothing in the combination of Nishizawa et al. and Mohindra et al., without the improper use of hindsight reconstruction, to motivate a person of ordinary skills in the art to arrive at the claimed method. Claim 11 respectfully is submitted as being patentable over Nishizawa et al. and Mohindra et al. Claims 63 and 70 are dependent on independent claims 61, and 68, respectively, discussed previously.

Claims 12, 15, 22, 25, 64, 67, 71, and 74 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nishizawa et al., in view of Hayami et al., U.S. Patent No. 5,474,616.

Claim 12 recites a method for "removing surface contaminants from an air/liquid interface of a semiconductor processing cleaning bath for processing semiconductor wafers." The method includes "reducing a volume of fluid in said semiconductor processing cleaning bath." This involves "rapidly removing from a processing apparatus an upper portion of a semiconductor processing fluid present in said bath, while said wafers are in said bath," which is accomplished "by hingedly releasing a door located at an upper portion of said bath to rapidly reduce an overall volume of processing fluid contained within said processing apparatus and to remove said surface contaminants from said air/liquid interface."

Nishizawa et al. lacks the requisite teaching of reducing a treatment fluid volume, as discussed above. Hayami et al. does not correct the deficiencies of Nishizawa et

al. Hayami et al. teaches a method for rinsing plate-shaped articles, such as semiconductor wafers, as well as cleaning equipment for the rinsing method. Significantly, Hayami et al. disclosed that folding walls 20 are folded to release treating fluid prior to immersion of the wafers. Hayami et al. does not teach or suggest removing a volume of treatment water "while said wafers are in said bath" as recited in the present claims.

Claims 12, 15, 22, 25, 64, 71, and 74 are submitted as being patentable over Nishizawa et al. and Hayami et al.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

Dated: April 28, 2003

Respectfully submitted,

By_____

Thomas J. D'Amico
Registration No.: 28,371
Peter McGee
Registration No.: 35,947
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorneys for Applicant